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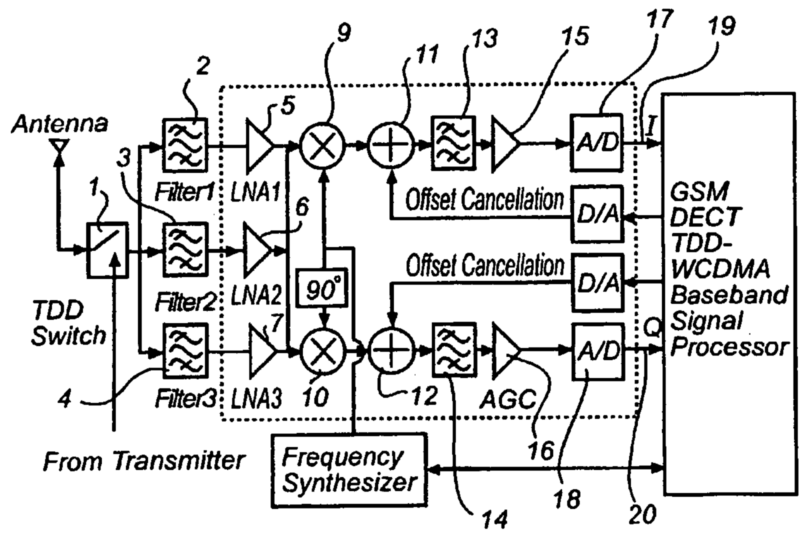
(54) Title: BASEBAND FRONT-END FOR MULTI STANDARD RECEIVER



(57) **Abstract:** The invention relates to a multi-standard receiver adopted to a plurality of wireless communication standards and comprising: receiving means; TDD switch means and a plurality of bandpass filter; a plurality of LNA means; mixer means; baseband analog processing means; analog-to-digital converter means, comprising a sigma-delta modulator, said converter means being hardware reconfigurable for different sampling frequency and different quantizing in dependence of different standard baseband signals; and a programmable decimation filter being programmable into different standard filtering modes for filtering different standard digital signals received from said analog-to-digital converter means, and comprising filter means being used in at least two different standard modes. The invention also relates to a baseband front-end device for a multi-standard receiver.

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BASEBAND FRONT-END FOR MULTI STANDARD RECEIVER

Technical field

The present invention relates generally to radio receiver architectures and analog-to-digital converters. More specifically, the invention concerns low power, high integration of radio frond-end for multi-standard and multi-mode communication systems.

Technical background

The proliferation of 2nd generation wireless and cellular standards and the imminent arrival of the 3rd generation cellular and satellite standard, has resulted in the development of many terminal architectures to the support wireless the TDMA (GSM), WCDMA (UMTS) and DECT wireless access methods. To ensure widespread acceptance and usage, it is important for timeliness to be capable of multi-standard operation, yet meet the commercial constraints of cost, size and power-consumption. One of the most critical points to overcome in multi-standard terminals for mobile and personal communication systems is to find the maximum number of commonalties to allow the highest possible degree of integration, under the constraints of low voltage and low power consumption. The starting point for multi-standard timeliness is to setup a common radio architecture capable to afford the various standards.

The most popular architecture of a radio subsystem is the so called "superheterodyne receiver". However this will developed receiver architectures require lots of external bandpass filters, such as high performance image rejection filter and IF channel selection filer, which are not amenable to integration and not cost effective for future production. To overcome the above limitations, the obvious way is to develop an architecture which is

more suitable for integration, in which the number of oscillators is reduced, and the IF functions (with associated passive filters) are suppressed, shifting the most important multi-standard operations to the baseband processing (preferable processed in low cost digital CMOS technology), of channel filtering and analog-to-digital processing.

Several radio receiver architectures are employed in the modern mobile terminal. These are superheterodyne receiver, low-IF receiver, zero-IF receiver and wide-band double-IF receiver. Each of them has its own prons and cons. Wide-band double-IF receiver has been investigated to be used in GSM/DECT multi-band receiver. This part briefly describes the state-of-the-art multi-standard receiver research.

The superheterodyne receiver remains the architecture of choice for the vast majority of RF applications in the world today. Its perennial popularity is due to its ability to reproducibly pick out narrow-bandwith high-frequency signals from the surrounding background clutter of signals outside the frequency range of interest. The RF signal is applied to a low-noise amplifier (LNA) and subsequently an image-reject filter. The combination of extremely high performance and low power requirement result in the LNA being one of the most significant power drains in the system. The image reject (IR) filter is typically implemented with a physically large surface acoustic wave (SAW) filter. In addition to their size, these filters have extremely unforgiving sensitivities to variations in source impedance, ground loops, and so on. The resulted signal from the IR filter is mixed with the output of a local oscillator (LO), thus producing the intermediate-frequency (IF) signal. The IF filter suppresses out-of-channel interferes, performing channel selection.

The principal issue in superheterodyne receiver is the trade-off between IR and adjacent channel suppres-

sion. For given filter quality factors (Qs) and losses, if the IF is high, the image is greatly attenuated whereas nearby interferes remain at significant levels. Conversely, if the IF is low, the image corrupts the downconverted signal but the interferes are suppressed. Another important drawback of heterodyne receivers is that the LNA must drive a 50 ohm load because the IR filter is placed off-chip. In terms of frequency plan, the superheterodyne architecture is not suitable for multistandard application. The multiple off-chip passive filter components are inevitable for different standards, which eliminates the possibility of a high-integration and low power terminal.

A Schematic diagram of a typical direct conversion receiver (DCR), also called homodyne or zero-IF-receiver, is shown in Figure 2. It is the natural approach to downconverting a signal from RF to baseband. A DCR translates the band of interest directly to zero frequency and employs low-pass filtering to suppress nearby interferes (adjacent channels). The quadrature I and Q channels are necessary in typical phase- and frequency-modulated signals because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases.

Direct conversion has several advantages over heterodyning. First the problem of image is circumvented bevause the IF is zero. Second, the LNA need not drive a 50ohm load because no image rejection filter is required. Third, the IF SAW filter and subsequent stages are replaced with low-pass filters (LPF´s) and baseband amplifiers that are amenable to monolithic integration and very low power consumption.

In the DRC, the LO frequency and the baseband low-pass filter can be made programmable to satisfy multiple communication standards. While the DRC approach is suitable for fully integration and can be easily made multi-

standard capable, several system level problems need to be overcome. In general, these problems are: DC offset, even-order distortion, 1/f noise and LO leakage back to antenna. All these offsets and low frequency noise should be removed either by analog feedback circuitry of adaptive digital cancellation. Different form the multi-band receiver, the multi-standard receiver should deal with signals of different bandwidth. For example, GSM family has 100 KHz baseband signal, DECT has 700 KHz baseband signal while WCDMA has 2.5 MHz baseband signal. This brings more difficulty on baseband filters and analog-to-digital converters for high integration multi-standard receiver.

The low IF receiver shown in Figure 3 converts the received RF signal to a low intermediate frequency whereby the on-chip bandpass filter can be used to perform channel selection. Though this architecture eliminates the problems of DC offset and 1/f noise associated with DRCs while maintaining the same level of integration, it reintroduces the image rejection. This time because of the rather low IF frequency, the image rejection is very difficult. Image rejection mixer techniques are required instead of image rejection filter, which is almost impossible to implemented in this situation. Also a bandpass filter or a bandpass sigma-delta modulator is needed to perform the channel selection and A/D conversion. Since give the same specifications, bandpass filter or modulator needs twice the number of poles and zeros comparing to it lowpass counterpart, the power consumption to achieve a wide bandwidth, such as WCDMA or DECT standard, becomes prohibitive.

An alternative architecture well suited for integration of the entire receiver is wideband IF with double conversion. Shown is Figure 4, this receiver system takes all of the potential channels and frequency translates them from RF to IF using a mixer with a single frequency local oscillator. A simple low-pass filter is used at IF

to remove any upconverted frequency components, allowing all channels to pass to the second stage of mixers. All of the channels at IF are frequency translated directly to baseband using a baseband filtering network where variable gain may be provided. This approach is similar to a superheterodyne receiver architecture in the frequency translation that is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscillator frequency translates all of the receive channels, maintaining a large bandwith signal at IF. The channel selection is the realized with the lower frequency tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multistandard-capable receiver features. This is essentially a dual downconversion heterodyne receiver, where the first downconversion employs an image reject mixer, and the second the homodyne approach.

The advantages of the architecture are that it eases the generation of the first local ocillator, which is now at a fixed frequency and that reradiation of the local oscillator back to the antenna is not a problem, as it would be if a direct downconversion technique were employed. This approach is highly desirable for monolithic integration, but suffers form the use of six high performance mixers to perform the complete downconversion, raising the DC power dissipation considerable. It also suffers from the same problem of existing homodyne receivers in terms of sensitivity to dc offsets and second-order distortion.

Summary of the invention

The object of this invention is to enable a receiver to efficiently handle several different wireless communication standards.

The object is achieved by a multi-standard receiver as well as a baseband front-end device according to the appended claims.

According to the invention a multi-standard receiver adopted to a plurality of wireless communication standards, comprises:

receiving means arranged to receive RF signals having different bandwidths;

TDD switch means and a plurality of bandpass filter means each adopted to a different standard, said TDD switch means being arranged to switch an incoming signal to a respective one of said plurality of bandpass filter means in dependence of the standard according to which the signal is transmitted;

a plurality of LNA means, each connected to a respective bandpass filter and adopted to a corresponding standard;

mixer means arranged to provide a baseband signal by downconverting the received signal directly to baseband centered at DC;

baseband analog processing means comprising filtering means for fixed standard specific filtering of the baseband signal and for standard specific automatic gain control;

analog-to-digital converter means, comprising a sigma-delta modulator, for providing a digital signal, said converter means being hardware reconfigurable for different sampling frequency and different quantizing in dependence of different standard baseband signals; and

a programmable decimation filter being programmable into different standard filtering modes for filtering different standard digital signals received from said analog-to-digital converter means, and comprising filter means being used in at least two different standard modes.

Further, according to the invention there is provided a baseband front-end device for a multi-standard receiver, the device comprising:

baseband analog processing means comprising filtering means for receiving and fixed standard specific filtering of a baseband signal and for standard specific automatic gain control;

analog-to-digital converter means connected to said baseband analog processing means, and comprising a sigma-delta modulator, for providing a digital signal, said converter means being hardware reconfigurable for different sampling frequency and different quantizing in dependence of different standard baseband signals; and

a programmable decimation filter being programmable into different standard filtering modes for filtering said digital signal received from said analog-to-digital converter means, and comprising filter means being used in at least two different standard modes.

The processing means operating at baseband frequency and being arranged for fixed standard filtering in combination with the programmable decimation filter provides for a simplified and efficient filtering operation for all standards involved. The use of a sigma-delta modulator arranged for different quantizing in dependence of the presently used standard additionally provides for an increased efficiency since different standards require differently advanced quantizing.

In an embodiment of the multi standard receiver according to this invention the programmable decimation filter comprises a multi-stage digital filter, with hardware sharing among different standards. This sharing simplifies the structure of the receiver and facilitates integration thereof.

Further objects and advantages of the present invention will be discussed below by means of exemplary embodiments.

Brief description of the drawing

Exemplifying embodiments of the invention will be described below with reference to the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of a prior art superheterodyne receiver;

Fig. 2 is a schematic block diagram of a prior art direct-conversion receiver;

Fig. 3 is a schematic block diagram of a prior art low-IF receiver;

Fig. 4 is a schematic block diagram of a prior art wideband dobuble-IF receiver;

Fig. 5 is a schematic block diagram of an embodiment of a receiver according to the present invention;

Fig. 6-9 show different portions of the receiver embodiment of Fig. 5 in more detail.

Description of embodiments

Referring now to Fig. 5-9 an embodiment of the receiver according to the present invention constitutes a zero-IF radio architecture for a TDD UMTS (WCDMA/GSM) with DECT-supportive terminal. Because of the TDD operation mode the terminal does not require simultaneous transmission and reception, thus a TDD switch can be used at the front-end instead of a duplexer. For a FDD UMTS terminal, the TDD switch should be replaced by a duplexer for WCDMA while the TDD switch is still needed for GSM and DECT.

First, narrow band tuned LNAs 5-7 are desired to save power and get high gain under the current sub-micron CMOS technology, which is preferred. Since the frequency operating bands for GSM, DECT and WCDMA cover from 1700 MHz to 2200 Mhz, three separated LNAs 5-7 will be needed, one for each standard. A TDD and Band selection switch 1 is provided after a receiving means, which here is embodied by an antenna. This switch is a single-pole-four-throw switch. The four throws are WCDMA receiver chain,

DECT receiver chain, GSM receiver chain and the transmission. This switch is controlled by the signal from the DSP controller chip, which is shown in Figure 6 as Standard-Switching Signal. This signal also controls the on-off statuses of the three LNAs 5-7 so that only one LNA is turned on when the receiver is operating. Considering the trade-off between dynamic range and sensitivity, it is preferable that every LNA 5-7 has switchable high gain and low gain mode.

As a Zero-IF receiver, the frequency of a local oscillator (LO), which is not shown per se but is comprised in a frequency synthesizer 8, should be the same as the center frequency of the desired signal. Thus the LO should also be switched among the three standards. Since the total frequency band of the receiver ranges from 1710 MHz to 1920 MHz, which is not too large for one voltage-controlled oscillator (VCO), it can be implemented either by one VCO or several VCOs for high phase-noise performance.

The receiver comprises an I mixer 9 and a Q mixer 10, which are shared by all the standards operation. Though highly-linear passive mixers in CMOS are successful, the importance of the combination gain of LNA and mixer, which should be sufficient to overcome the flicker and thermal noise of the baseband stages, makes lossy passive mixers out of the consideration in zero-IF receiver. Each mixer 9 and 10 respectively is followed by a respective series of an adder 11 and 12, a baseband filter 13 and 14, an AGC unit 15 and 16, and an A/D converter 17 and 18. To reduce the relative importance of the noise which is inevitably introduced by the baseband filter 13/14 and the AGC unit 15/16, around 10dB gain is required in the mixer 9/10. To handle in-band blocking as well as intermodulating signals the mixer also needs to achieve more than -3dBm of IIP3.

As is evident from above, the baseband processing includes filtering and AGC, which could be regarded as

being performed in a baseband filter, which can be implemented by a gm-C, a MOSFET-C, or an RC active architecture. In the architecture of this embodiment, the baseband filter should be designed to satisfy the WCDMA standard, which requires a bandwidth of approximately 2.5 MHz taking the channel spacing into account. Thus the channel filtering of WCDMA standard is accomplished. The filtering characteristic is fixed, since, in GSM and DECT modes it is not necessary to alter the characteristic of this filter. The channel filtering of GSM and DECT standards is realized after the analog-to-digital converters 17, 18. There are two branches 19, 20 for I and Q channels. The effect of the baseband filter in GSM and DECT modes is that it acts as a anti-aliasing filter. Further, the filter can be switched into a low power mode in GSM and DECT operations

Figure 7 presents one architecture of the baseband processing to be used in both branches. The input differential signals are the downconverted ones from the mixer 9 or 10. In this embodiment the whole fixed baseband filter 13 and 15 or 14 and 16 is divided into several blocks 21-25 having the function of either filtering or amplification. An anti-aliasing filter 21 is used to filter out the noise and blockers outside of the sampling frequency of the analog-to-digital converter 17/18 in WCDMA operation. A combination of a first filter section 22, which follows the aniti-aliasing filter 21, and a second filter section 24 has enough attenuation on the blockers according to WCDMA standard. 6^{th} or higher order filtering, for example by means of a 6^{th} order Butterworth filter, is required for complying with WCDMAchannel filter specifications based on adjacent channel interference and blockers. Amplifiers VGA1, 23, provided between the first filter section 22 and the second filter section 24, and VGA2, 25, following the second filter section 24, realize the AGC function so that the enough dynamic range can be achieved, which in this embodiment is set to be

32dB to 80dB range for all the standards. The interleaving of filtering and VGA helps to get the required IIP3 specification of the whole receiver.

Analog-to-digital converter (ADC) is an important part of the receiver. It makes the multistandard receiver efficient and low power. As mentioned in the previous part, only WCDMA channel filtering is realized in the baseband analog processing. The filtering of the baseband circuits has almost no attenuation on the blockers. So for GSM and DECT standards, the ADC needs much higher dynamic range (resolution) comparing with WCDMA standard. A high performance sigma-delta modulator ADC is used in the receiver in accordance with this embodiment, as shown in Fig. 8. By changing the sampling frequency, the A/D converter can be easily set to have at least 14-bit, 12-bit, or 7-bit resolution for three different standards, and thus, in a sense, it is easily hardware reconfigurable.

Figure 8 shows the sigma-delta modulator architecture, which is a 2-2 cascaded sigma-delta modulator. Thus, the architecture has two 2nd order switched-capacitor modulators 26, 27 in cascade in order to guarantee stable operation with all inputs. To improve the dynamic range of the WCDMA/DECT operating mode, a 3-bit quantizer, realised by means of a 3-bit DAC feedback 28, is used. The quantization noise can be decreased by 18dB. In the GSM mode, however, a 1-bit quantizer 29 is used, rather than the 3-bit quantizer 28, at the second stage to save power. Thus, the ADC is switchable between the two different quantizing operations, and the hardware of the sigma-delta modulator is reconfigurable accordingly. The mode is controlled by the static switch signal S fed to switches 32 and 33, which switch between the 1-bit and 3-bit quantizers at the input and output ends respectively of the quantizers 28, 29. All the building blocks can be shared for three modes, saving both chip area and power consumption. The outputs of the 3-bit and 1-bit

quantizers 28, 29 are encoded in 2's complement before fed to digital error cancellation logic 30. The frequencies of the sampling signal in the figure are 13 MHz, 26 MHz and 39 MHz for GSM, DECT and WCDMA respectively. Together with the second-stage quantizer switching, this guarantees that enough dynamic ranges are obtained by the ADC for the signals of GSM, DECT and WCDMA, which are 90 dB, 75 dB and 46 dB. Other techniques are used to further decrease the power consumption. Capacitor scaling in the first stage integrator 31 can greatly reduce the power consumption for DECT and WCDMA while the same OTA, with low power biasing, is used. The fourth stage integrator 34 gain coefficient is switched so that the range of the 3-bit quantization can be fully exploited, thus get higher resolution for DECT and WCDMA.

To achieve a multi-standard receiver, a programmable decimation filter is needed, as shown in Figure 9.

It is a multi-stage decimation filter. It consumes much less power and saves much area in comparison with the one-stage realization. For GSM standard, the oversampling ratio of the sigma-delta modulator is 64. The 13 Msps signal is downsampled by two sinc filters 35, 36 and two half-band filters 37, 38. For DECT standard, the oversampling ratio is 16. The 26 Msps signal is downsampled by one sinc filter 36 and two half-band filters 39, 40. For WCDMA, the oversampling ratio is 8. The 39 Msps signal is downsampled by one sinc filter 36 and one half-band filter 39. In Figure 9, one sinc filter 36 is shared by signals of all the standards and one half-band filter 39 is shared by DECT and WCDMA standards.

The receiver architecture according to the present invention is easy to fully integrate. The receiver has smallest number of building blocks, and thus it consumes very low power.

Further, it is a true multi-standard receiver that can deal with the signals with different bandwidth in the baseband. Though the example of this invention is used

for WCDMA/GSM/DECT, the idea can be easily extended to more standards, like Bluetooth, HomeRF, PDC and IS95 without much architecture change and circuit level redesign.

The baseband analog filter is designed for the widest standard (WCDMA). No strictly specified analog filter with 100KHz bandwidth is needed for narrow band standard (GSM), thus the huge chip size of capacitors and resistors used in the filter, which could be prohibitive for integrated circuit, is avoided.

The sigma-delta modulator as the ADC easily solves the problem of different bandwidth and different resolution of the different standards. The hardware reconfigurability in the modulator enables the full dynamic range and speed for all the standards in this proposed receiver architecture.

The programmable decimation filter moves the complex analog signal processing to the digital domain, whereby the processing is simplified. Especially for the GSM standard, the accurate filter characteristics can be completed without any difficulty, which can be hardly realized if an analog filter is employed because of the process variation in integrated circuits. The multi-stage decimation filter enables the maximum circuit sharing for all standards resulting in a substantial saving of the chip area and power consumption.

CLAIMS

1. A multi-standard receiver adopted to a plurality of wireless communication standards, and comprising:

receiving means arranged to receive RF signals having different bandwidths;

TDD switch means and a plurality of bandpass filter means each adopted to a different standard, said TDD switch means being arranged to switch an incoming signal to a respective one of said plurality of bandpass filter means in dependence of the standard according to which the signal is transmitted;

a plurality of LNA means, each connected to a respective bandpass filter and adopted to a corresponding standard;

mixer means arranged to provide a baseband signal by downconverting the received signal directly to baseband centered at DC;

baseband analog processing means comprising filtering means for fixed standard specific filtering of the baseband signal and for standard specific automatic gain control;

analog-to-digital converter means, comprising a sigma-delta modulator, for providing a digital signal, said converter means being hardware reconfigurable for different sampling frequency and different quantizing in dependence of different standard baseband signals; and

a programmable decimation filter being programmable into different standard filtering modes for filtering different standard digital signals received from said analog-to-digital converter means, and comprising filter means being used in at least two different standard modes.

2. A multi-standard receiver according to claim 1, said filtering means of said baseband analog processing means comprising a filter structure having an at least 6-order filtering characteristic and a variable gain ampli-

fier, wherein said filtering characteristic is fixed for the standard with widest signal bandwidth.

3. A multi-standard receiver according to claim 1 or 2, said plurality of wireless communication standards comprising at least one of GSM, DECT and WCDMA standard.

4. A multi-standard receiver according to anyone of the preceding claims, wherein said sigma-delta modulator is arranged as a 2-2 cascaded architecture, constituted by a first and a second stage, and comprises, at the second stage, a 1-bit quantizer, a 3-bit quantizer and a switching mechanism connected to said quantizers, said switching mechanism being operable for switching between said quantizers for obtaining said different quantizing.

5. A multi-standard receiver according to anyone of the preceding claims, wherein said programmable decimation filter comprises a multi-stage digital filter, with hardware sharing among different standards.

6. A baseband front-end device for a multi-standard receiver, the device comprising:

baseband analog processing means comprising filtering means for receiving and fixed standard specific filtering of a baseband signal and for standard specific automatic gain control;

analog-to-digital converter means connected to said baseband analog processing means, and comprising a sigma-delta modulator, for providing a digital signal, said converter means being hardware reconfigurable for different sampling frequency and different quantizing in dependence of different standard baseband signals; and

a programmable decimation filter being programmable into different standard filtering modes for filtering said digital signal received from said analog-to-digital converter means, and comprising filter means being used in at least two different standard modes.

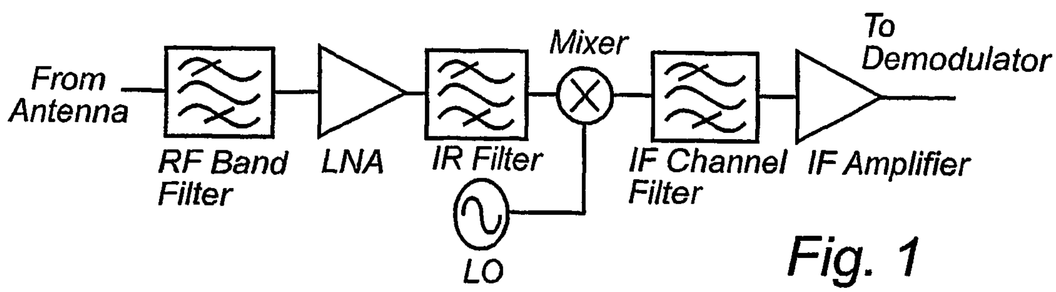


Fig. 1

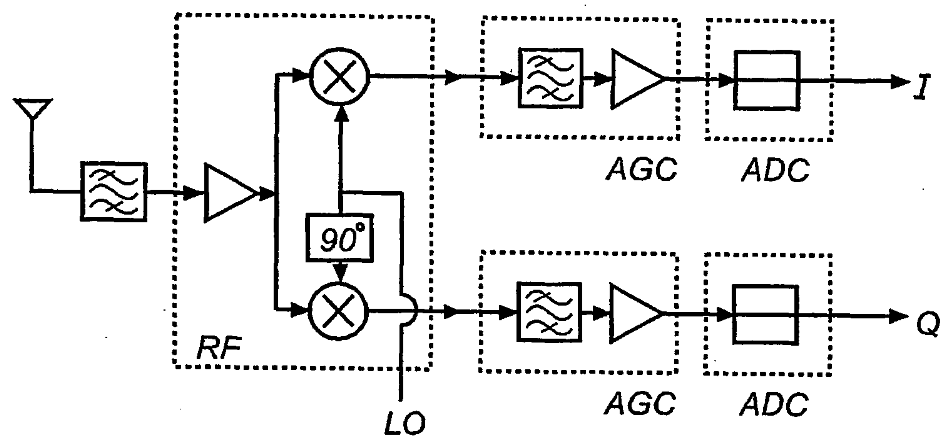


Fig. 2

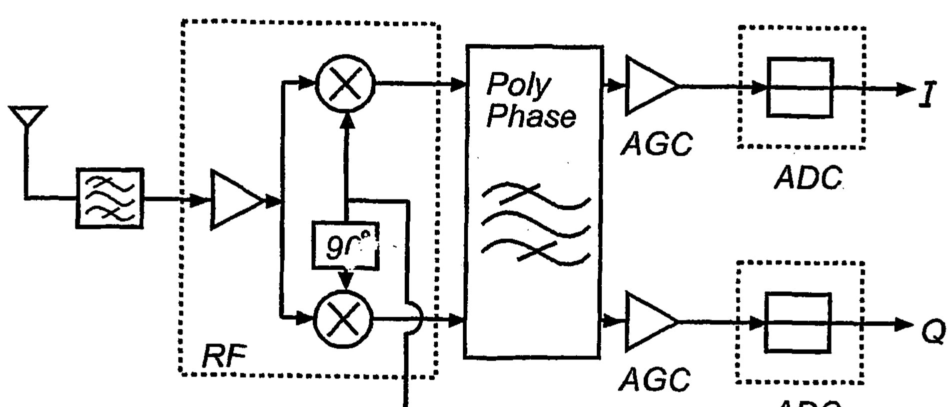
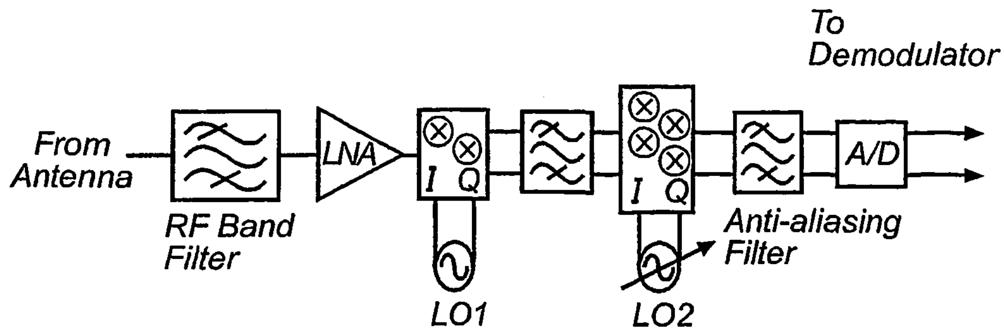


Fig. 3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From Antenna
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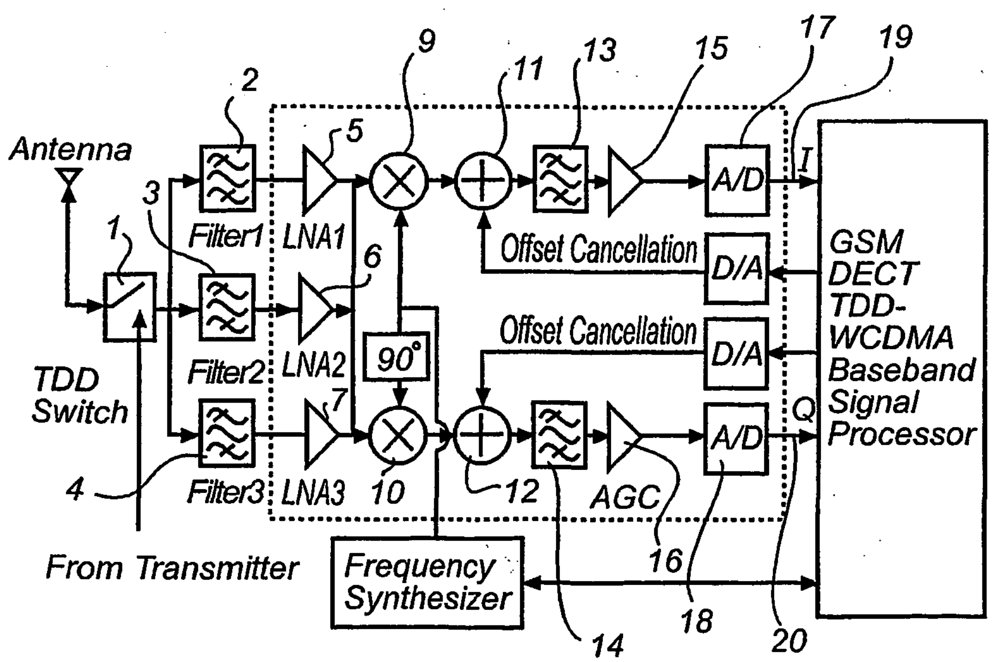
A/D
RF Band Filter
Anti-aliasing Filter
LO1
LO2

Fig. 4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From Transmitter
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Filter2
Filter3
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LNA2
LNA3
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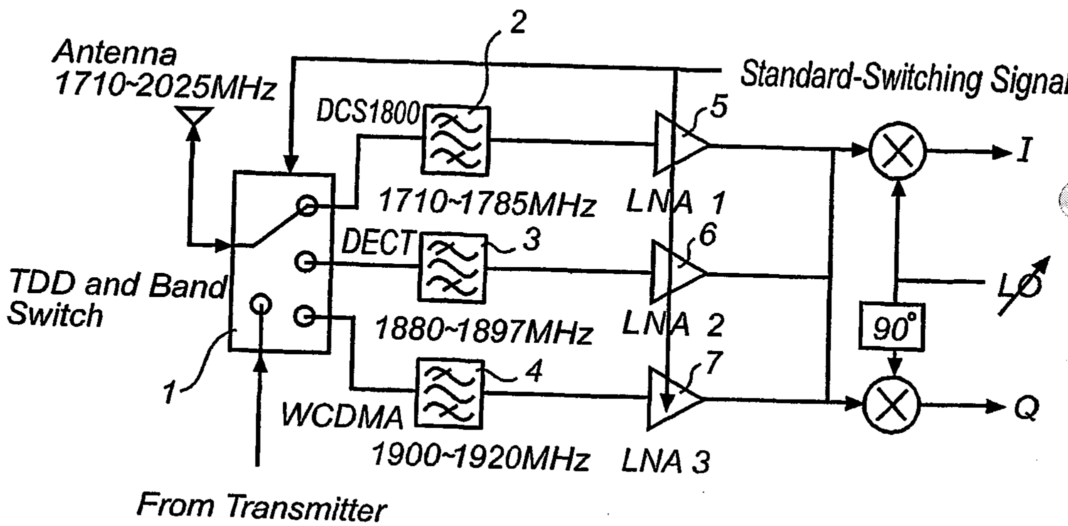
D/A
D/A
A/D
A/D
AGC
I
Q
Frequency Synthesizer
GSM DECT TDD-WCDMA Baseband Signal Processor
1
2
3
4
5
6
7
9
10
11
12
13
14
15
16
17
18
19
20

Fig. 5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DCS1800
5
I
1710~1785MHz
LNA 1
DECT
3
6
TDD and Band
Switch
LO
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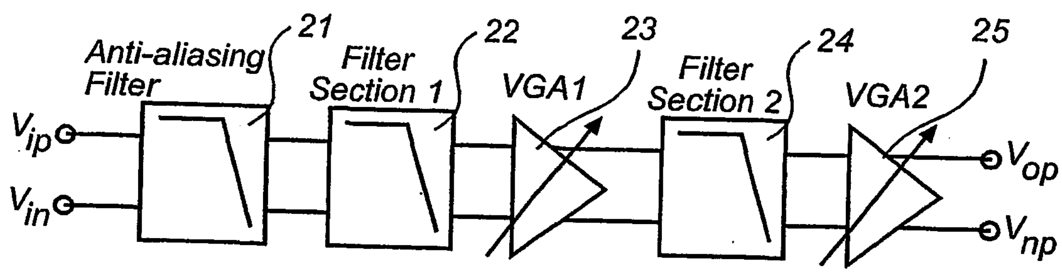
LNA 2
7
1
4
WCDMA
Q
1900~1920MHz
LNA 3
From Transmitter

Fig. 6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21
Filter
Section 1
22
VGA1
23
Filter
Section 2
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VGA2
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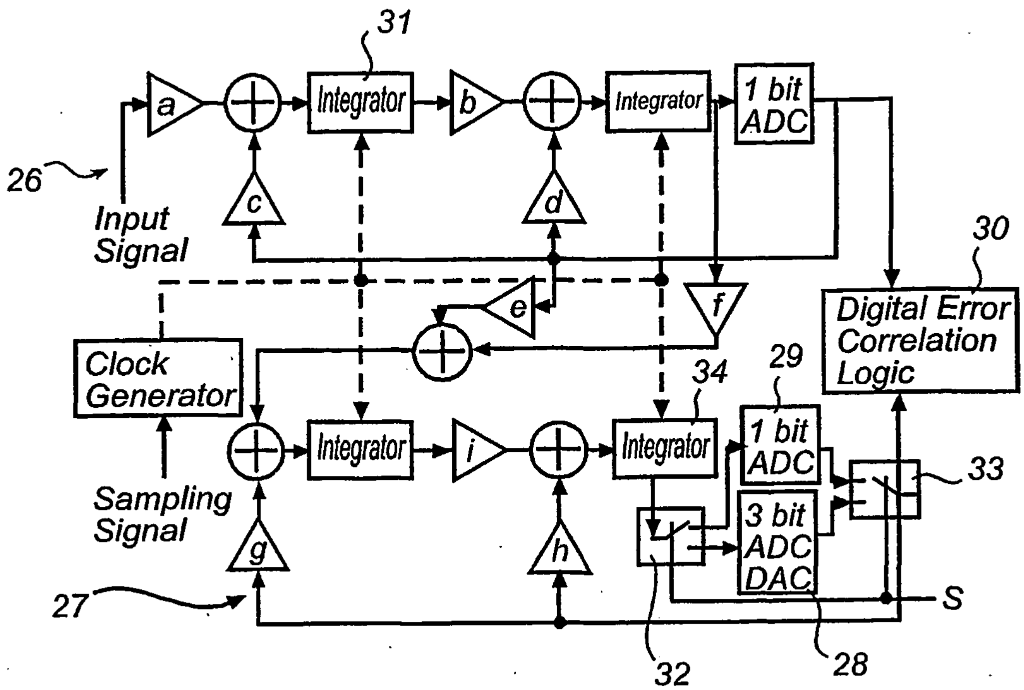
V_{np}

Fig. 7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Integrator
1 bit
ADC
26
Input
Signal
30
Digital Error
Correlation
Logic
Clock
Generator
34
29
Integrator
1 bit
ADC
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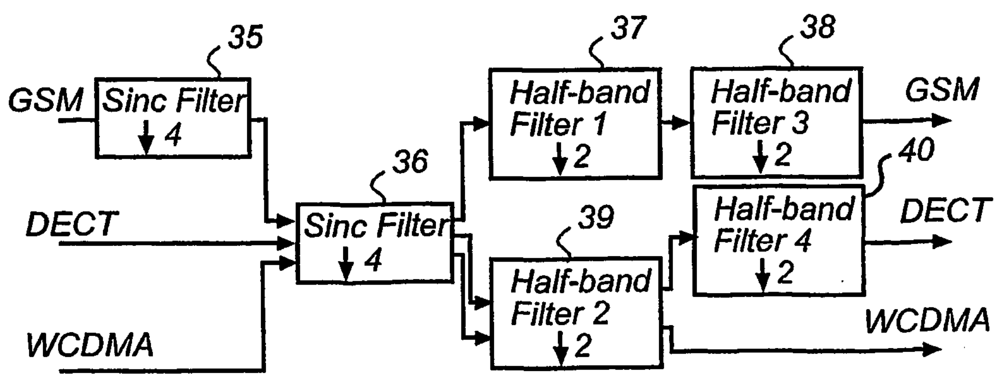
Sampling
Signal
3 bit
ADC
DAC
S
27
32
28

Fig. 8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GSM
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↓4
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Filter 1
↓2
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Filter 3
↓2
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40
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DECT
Sinc Filter
↓4
39
Half-band
Filter 4
↓2
DECT
Half-band
Filter 2
↓2
WCDMA
WCDMA

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/02114

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H04B 1/16, H03M 3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H04B, H03M, H03H, H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI DATA, EPO-INTERNAL, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	W-CDMA: aspects of implementation Kourtis S; McAndrew, P.; Tottle, P. Semicond. Products Sector, Motorola, UK This paper appears in: UMTS-The R&D; Challenges (Ref. No. 1998/496) IEE Colloquium on On page(s): 10/01-10/8 23 Nov. 1998 INSPEC Accession Number: 6169013 se sidan 5 - sidan 8 och figurer 3 och 4 --	1-6
Y	WO 0041322 A1 (INFINEON TECHNOLOGIES AG), 13 July 2000 (13.07.00), page 1, line 2 - page 6, line 5 --	1-6

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 December 2001

Date of mailing of the international search report

15-01-2002

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/02114

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Multi-standard DSP based wireless system Kuo, C.; Wong, J. Signal Processing Proceedings, 1998. ICSP 1998 Fourth International Conference on On pages(s): 1712-1728 vol. 2 12-16 Oct. 1998 INSPEC Accession Number: 6370782 se sidan 1714 - sidan 1728 --	1-6
A	WO 0051376 A1 (TELEFONAKTIEBOLAGET LM ERICSSON), 31 August 2000 (31.08.00), page 1, line 6 - page 10, line 29 -- --------	1-6

INTERNATIONAL SEARCH REPORT
Information on patent family members

06/11/01

International application No.
PCT/SE 01/02114

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0041322 A1	13/07/00	EP 1142144 A	10/10/01
WO 0051376 A1	31/08/00	AU 3340400 A	14/09/00
		AU 4303399 A	06/12/99
		BR 9910572 A	16/01/01
		EP 1073946 A	07/02/01
		SE 9900719 A	27/08/00

Form PCT/ISA/210 (patent family annex) (July 1998)